1   VIDEO DISTRIBUTION SYSTEM AND METHOD

2

3   RELATED PATENTS/APPLICATIONS

4   The present application is related to the patent application/patent having serial/patent

5   number *****, entitled, "MULTI-MODE VIDEO PROCESSOR" by Meddaugh et al., filed

6   concurrent herewith on December 15, 2000 and which is incorporated herein by reference.

7

8   FIELD OF THE INVENTION

9   The present invention generally relates to the distribution of video signals from

10   multiple sources. More particularly, the invention relates to an integrated and modular video

11   signal distribution and control system.

12

13   BACKGROUND

14   With the arrival of digital video technology and economical hardware, new

15   applications are conceived and deployed with increasing regularity. Digitizing video signals

16   enables remote and selective monitoring of one or more video signals, and economical

17   hardware increases the range of problems for which the technology is suitable for

18   applications.

19   Some digital video applications involve multiple personnel monitoring selected ones

20   of a number of video signals. In these applications, the number of personnel is usually less

21   than the number of video signals, processor-based control allows concurrent display of one or

22   more video signals at a display terminal, and each person monitors and controls the display at

23   one or more display terminals. For example, 4 people may be assigned the task of monitoring

24   the video signals from a dozen or more sources, wherein each person can select for display at

25   a display terminal one or more of the video signals. It will be appreciated that such systems

26   have use in security, military, aviation, traffic, environmental and many other applications.

27   The particular requirements related to weight limits, modularity, and fail-safe

28   operations present many challenges for designers of video distribution system. For example

29   in a distributed architecture, workstations with powerful hardware and complex software may

30   perform functions related to digitizing video signals and controlling the distribution and

31   display of the video data. The distributed architecture may be excessive in terms of cabling if

1 weight is a consideration and may be unduly complicated if modularity is a consideration.

2 Another challenge involves adapting custom designed video distribution systems and

3 applications to use commercial off the shelf (COTS) parts versus custom designed parts.

4 Many manufacturers prefer to manufacture high volume parts and charge a premium to

5 provide low volume, custom parts. To further complicate the situation for system designers,

6 the output pin resources provided by COTS parts are also reduced at a time when system

7 users are demanding that the video distribution system support more video channels. A

8 system and a method that addresses the aforementioned problems, as well as other related

9 problems, are therefore desirable.

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11 SUMMARY OF THE INVENTION

12   The present invention is an integrated video distribution system for distributing video

13 signals from a plurality of sources. In one embodiment, the system includes a digitizer

14 arrangement arranged and configured to receive analog video signals from a plurality of video

15 sources. The analog video signals are digitized to YCrCb format, multiplexed and converted

16 to streams of digital video data that are transmitted on a digital video bus having a plurality of

17 video channels. In one embodiment, the digitizers and video bus are integrated with a

18 backplane arrangement that includes expansion slots for a plurality of terminal controllers.

19 The expansion slots provide connections to the video bus. Each terminal controller mounted

20 on the backplane arrangement can be coupled to a display terminal and an input device. The

21 terminal controller selects one or more of the input streams of video data in response to

22 control signals from the input device and converts the selected video data to an analog video

23 signal for output to a display terminal. This arrangement provides a compact, yet modular

24 and expandable video distribution system.

25   In another embodiment, a fail-safe video subsystem is coupled to the output ports of

26 the terminal controllers. The fail-safe video subsystem has additional input ports for one or

27 more video signals from alternative video sources. When power is applied to the fail-safe

28 video subsystem, the input video signals are selectable for output, and when power is not

29 applied, the video signals from the alternative sources are output.

30   It will be appreciated that various other embodiments are set forth in the Detailed

31 Description and Claims that follow.

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2   BRIEF DESCRIPTION OF THE DRAWINGS

3   Various aspects and advantages of the invention will become apparent upon review of

4   the following detailed description and upon reference to the drawings in which:

5   FIG. 1 is a block diagram of a video distribution system;

6   FIG. 2 is a block diagram of a video distribution and control arrangement in

7   accordance with one embodiment of the invention;

8   FIG. 3 is a functional block diagram of digitizer in accordance with another

9   embodiment of the invention;

10   FIG. 4 is a functional block diagram of an example fail-safe video module;

11   FIG. 5 is a circuit schematic for one color (e.g., of RGB) of station 0 of a multiplexer-

12   and-relay module which is in an energized state; and

13   FIGs. 6A and 6B are circuit schematics for one color (of RGB) of stations 1-8 of an

14   example multiplexer-and-relay module having 9 stations and which is in an energized state.

15

16   DETAILED DESCRIPTION

17   In various embodiments, a video distribution and control system and method are

18   provided in which video signals from analog and digital sources are input to a digitizer

19   arrangement. The digitizer arrangement digitizes the analog video signals into video data,

20   formats the video data for compatibility with a standard video bus, and multiplexes the video

21   signals over the video bus. The video bus is integrated with a backplane arrangement, which

22   has slots available for a plurality of terminal controllers. Each of the terminal controllers is

23   associated with a display terminal and an input device, and video data from the video bus are

24   selectively converted to an analog video signal for the display terminal responsive to control

25   signals from the input device. The centralized digitizer arrangement, which is integrated with

26   the backplane, supports modular expansion for adding display terminals and also reduces

27   cabling. In one embodiment, the backplane and associated terminal controllers are contained

28   and mounted within a single cabinet that is suitable for electronic equipment. A single power

29   supply powers the arrangement. This arrangement provides a compact, yet modular and

30   expandable video distribution system.

1   In another embodiment, video signals from fail-safe sources are input to the system.

2   The fail-safe sources comply with selected fail-safe criteria, and the fail-safe video signals are

3   made available at the display terminals, even if the digitizer and distribution arrangement

4   fails.

5   FIG. 1 is a block diagram of a video distribution system. System 100 receives video

6   signals from a plurality and variety of sources. Various combinations of one or more of the

7   video signals are then selectively routed and displayed at display terminals. System 100

8   includes centralized video distribution and control arrangement 102 and a plurality of

9   terminals. Each of the terminals includes an input device (104-1 - 104-*n*) and a video display

10   terminal (106-1 - 106-*n*), each of which is driven by a separate video signal from video

11   distribution and control arrangement 102.

12   Video distribution and control arrangement 102 receives video signals from a plurality

13   of sources, which may include video cameras that generate NTSC signals, digital video

14   cameras that generate digital video data, or radar systems, for example. The analog video

15   signals are digitized within distribution and control arrangement 102 for the purpose of

16   selecting video stream(s) and combining selected video data with graphical overlay data in

17   response to signals from one of input devices 104-1 - 104-*n*. Digital video data that is input to

18   the distribution and control arrangement is also selectable by the terminals. Operationally, for

19   example, there may be 10 video sources, and 4 of the video sources may be selected for

20   display at a particular one of the display terminals 106-1 - 106-*n*. The selection of the video

21   sources is made in response to control signals received from the input device that is associated

22   with the particular display terminal. Video distribution and control arrangement 102 converts

23   the selected and combined digital video data to an analog video signal (e.g., RGB) to drive a

24   video display.

25   The selection of video streams for display at a display terminal is user-controlled via

26   an associated input device. An input device may take various forms, depending on

27   application requirements. For example, input device may be a keyboard, a mouse, trackball,

28   voice control or other known apparatus. Alternatively, the input device could be a separate

29   touch screen or integrated with the display terminal in the form of a touch screen. In addition,

30   numerous software control methodologies (commands, menus, and GUIs) could be employed

31   in supporting the selection.

1   The overlay of graphical data onto video data is also performed in response to user

2   controls initiated at an input device. For example, textual data can be overlaid on video data

3   from a radar source for coordinate and directional information.

4   Although display terminals 106-1 - 106-*n* are all illustrated as being of the same type,

5   it will be appreciated that different combinations of types of video display terminals could be

6   used. For example, various combinations of monochrome and color display terminals, as well

7   as various gradations thereof, could be used. Thus, the respective digital-to-analog converters

8   of video distribution and control arrangement 102 must be compatible with the type of display

9   terminal.

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11   FIG. 2 is a block diagram of a video distribution and control arrangement in

12   accordance with one embodiment of the invention. Video distribution and control

13   arrangement 102 receives a plurality of analog video signals, digitizes the signals into digital

14   video streams, and selects subsets of the video streams for display on the connected video

15   displays. In addition, graphical data generated in response to control signals from the input

16   device are overlaid on the video data.

17   Video distribution and control arrangement 102 includes digitizer 152, multiple

18   terminal controllers 154-1, 154-2, 154-3, ... 154-*n* and fail-safe video module 156. Digitizer

19   152 includes multiple analog-to-digital converters that generate digital video data from the

20   input video signals and drives the video data on digital video bus 158. The video data that is

21   generated from a particular video signal is referenced herein as a "video stream". Each

22   terminal controller 154-1 - *n* performs the function of selecting one or more video streams for

23   display on a connected display terminal in response to signals from a connected input device.

24   For example, control signals are received by terminal controllers 154-1 - 154-*n* on lines 155-1

25   - 155-*n*. In addition, the terminal controller overlays graphics data on the video data in

26   accordance with input signals and software executing within the controller.

27   Video bus 158 is comprised of a plurality of individual video buses (not shown), each

28   dedicated to one of the video streams. Thereby, each of the terminal controllers 154-1 - 154-*n*

29   has access to all of the video streams. In one embodiment, the individual buses include either

30   8 data lines and two clock lines (10-line buses) or 8 data lines and a single clock line (9-line

31   buses). The 10-line buses may be used to carry either one color or two monochrome video

1   streams. The data from the various sources is multiplexed on the buses to reduce the number

2   of lines.

3   In an example embodiment, control bus 160 is implemented as a standard

4   VersaModule Eurocard bus (VME bus). Control bus 160 is used to set various control

5   registers in the modules that are connected to the bus. For example, digitizer 152 has control

6   registers that dictate which video streams are carried on which of the video buses 158,

7   terminal controllers 154-1 - *n* have control registers that control which video buses are routed

8   to display presentation processing elements (within the terminal controller) and thereafter to

9   up to four independent display terminals, and fail-safe video module 156 has control registers

10   that are used for selecting between fail-safe video signals and the other video signals. It will

11   be appreciated that system-level control can be accomplished with an additional processor

12   (not shown) that is coupled to control bus 160 for configuring the control registers of digitizer

13   152, terminal controllers 154-1 - 154-*n*, and fail-safe video module 156.

14   Video bus 158 and control bus 160 are integrated with backplane arrangement 162,

15   which includes card slots (not shown) into which terminal controllers 154-1 - 154-*n* can be

16   inserted. Thus, a modular system is provided in which additional display terminals 106 and

17   accompanying input devices 104 can be added to the system with "plugable" terminal

18   controllers and appropriate cabling. The backplane is comprised of a printed circuit board

19   having signal lines for the control bus and video bus, components mounted on the circuit

20   board to implement digitizer 152, and card slots for connecting terminal controllers. The card

21   slots conform to ANSI/VITA standard 1-1994 (American National Standard for VME64), for

22   example.

23   Terminal controller 154 performs the functions of selecting video streams from video

24   bus 158 in response to user-control signals from an input device and converting the video

25   streams from digital signals to analog signals. In addition, graphics data is overlaid on the

26   video streams in accordance with application processing requirements.

27   Fail-safe video module 156 is provided to supply video signals from fail-safe sources,

28   even if digitizer 152 or the sources supplying video signals thereto fail. For example in a

29   security application, battery powered video cameras could be employed for scenarios where

30   power is lost to other video sources. The particular characteristics of the fail-safe video

31   sources are determined by the application. Module 156 provides video signals to the system

1   display terminals 106-1 - 106-*n*, wherein the particular video signals that are output are either

2   the video signals on lines 164 from the fail-safe video sources or the video signals from the

3   terminal controllers 154-1 - 154-*n*. A set of relays is used to provide a specific video signal

4   path even when the module is not energized (in the absence of power). In one embodiment,

5   fail-safe video module 156 drives a plurality of RGB video outputs and also has a plurality of

6   RGB inputs. Each of the video outputs has a fail-through capability, wherein video signals

7   pass through the relays when the relays are in a de-energized state.

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9   FIG. 3 is a functional block diagram of digitizer 152 in accordance with one

10   embodiment of the invention. Digitizer 152 receives both analog and digital video signals and

11   generates digital video streams that are driven on the video buses 158.

12   Video input matrix 202 has input ports for 5 NTSC composite video signals and two

13   S-video signals. The two S-video ports can also be used for a single NTSC composite video

14   signal and are together referenced as input port 0, and the remaining input ports are referenced

15   as input ports 1-5. The output ports of input matrix 202 are labeled to correspond to the input

16   port numbers. Signals on input ports 0 and 1 are routed to digitizer 0; signals on input ports 1

17   and 2 are routed to digitizer 1; signals on input ports 2 and 3 are routed to digitizer 2; signals

18   on input ports 3 and 4 are routed to digitizer 3; and signals on input ports 4 and 5 are routed to

19   digitizer 4. Input matrix 202 is implemented with a set of analog multiplexers that route the

20   video signals as indicated. While input matrix 202 is shown as having 5 composite video

21   input ports and 2 S-video input ports, it will be appreciated that different combinations of

22   various types of video input ports could be used in alternative embodiments.

23   Each of digitizers 0-4 convert NTSC/EIA-170 video signals to digital format, for

24   example, 8-bit YCrCb 4:2:2 format video data. Each digitizer has four multiplexed video

25   input ports, of which 3 ports are used. For systems having additional video sources and

26   additional video buses 158, the fourth input port of a digitizer may be used. Each digitizer

27   selects the video signal from one of the input ports and generates digital video data for the

28   selected signal.

29   Each digitizer selects from three input video signals. Two of the input video signals

30   are the signals provided by input matrix 202 from the various video sources, and the third

31   video signal is from video test generator 230. It can be seen that the video signals from input

1   ports 2-4 of matrix 202 are output to two digitizers. For example, the signal from port 1 is

2   input to digitizers 0 and 1. This provides a level of redundancy for the signals on ports 1-4

3   relative to the digitizers. That is, if digitizer 0 fails, the signal from port 1 can still be

4   digitized by digitizer 1. No redundancy is provided for ports 0 and 5.

5   Each of the digitizers has 16 output signal lines and converts the signal into a YCrCb

6   digital video format. In the example embodiment, digitizers 0-4 are implemented with

7   Brooktree BT 829 model digitizers.

8   Analog source video controller 204 receives input video streams from digitizers 0-4

9   and converts the video data to VIDbus2 format. Controller 204, in response to control signals

10   received via local bus 206, also selectively places any of the output signals from digitizers 0-4

11   in various combinations on the five VIDbus2 buses 0-4, utilizing a full VIDbus for color

12   video data or half a VIDbus for monochrome data.

13   Prior video distribution systems had on the order of 300 pins available for distribution

14   of video signals. Since an RGB video signal requires 7 bits per color plus control bits, 24 bits

15   per channel are typically required. If the user requires 6 channels, the number of pins requires

16   increases to 144 (6 channels * 24 bits). However, where cost constraints dictate the usage of

17   generally available VME bus connectors having fewer than 100 pins and the demand for

18   video channels is increasing, the challenge faced is that of having too few pin resources to

19   meet the output demanded of the video distribution system. To solve this problem, the analog

20   signals are digitized in YCrCb format and the video data multiplexed over the available

21   channels.

22   The video data that is output from video controller 204 is input to bus drivers 0-4 on

23   three 10-bit and two 9-bit channels. The 10-bit channels can be used for a single color video

24   stream (8 data lines and two clock lines) while the 9-bit channels are used only for color video

25   streams (8 data lines and one clock line). However, to reduce the number of lines from the

26   bus drivers, the bus driver outputs are multiplexed via a VID Bus Multiplexer (not shown)

27   from video buses 158.

28   Video data is received by analog video controller 204 from digitizers 0-4 at a clock

29   rate that is twice the output of controller 204. At controller 204 the data is clocked at a rate of

30   up to 33 MHz with two data words being transmitted during a single clock cycle (the first

31   word on the rising clock edge and the second word on the falling clock edge). Using double

1   edge clocking effectively reduces the number of lines and reduces the clock speed from video

2   controller 204 to the MMVP (Multimode Video Processor – not shown), thereby avoiding

3   frequency mismatch problems or glitching that may occur on backplane 162 due to the use of

4   off the shelf components. All data lines should be stable at least 4ns before a clock edge is

5   measured. All data lines should also be held valid for a minimum of 0ns after a clock edge is

6   measured. The data is latched and demultiplexed so that is it provided on router data lines

7   (not shown) at 1/2 the incoming rate (where first and second data words are available at rising

8   clock edges). Thus the decoding of the data at the MMVP module (not shown), coupled to

9   VID 152, is automatic by using the appropriate edge to clock the data into each half of the

10   data register.

11   In an example embodiment, VID buses 0-2 consist of a 10-signal interface wherein the

12   upper half of the 10-signal interface includes 4 data lines and an associated clock line, and the

13   lower half is similarly arranged. The number of input pins is reduced by time multiplexing

14   pixel data on each half of the bus using the rising and falling edges of the clock signal. Four

15   bits comprising half of word 0 are transferred on the rising edge of the clock, and four bits

16   comprising half of word 1 are transferred on the falling edge of the clock. Thus, each

17   complete clock cycle produces 8 bits of data from each half of a VID bus. When both halves

18   of a transfer are used together, a single color video stream can be transferred on a VID bus.

19   VID buses 3-4 are comprised of 9 signal lines: 8 data lines and 1 clock line. Thus, as

20   compared to the 10-wide VID buses the 9-wide VID buses have a single clock signal

21   controlling both the upper and lower halves of the 8 data lines. The tables below illustrate the

22   color and monochrome data formats. Table 1 is the data format for a 10-wide VID bus

23   configured for a single color video stream; and Table 2 is the data format for a 9-wide VID

24   bus configured for a single color or monochrome video stream. Note that Table 1 includes

25   two clock signals (C(U) and C(L)), while Table 2 includes only a single clock signal. Y0-7

26   are the bits that represent the intensity level of a pixel, and CrCb0-7 represent the chroma

27   level of a pixel.

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Video stream A   Video stream B

line	C(U)	7	6	5	4	C(L)	3	2	1	0
word 0	rising	CrCb3	CrCb2	CrCb1	CrCb0	rising	Y3	Y2	Y1	Y0
word 1	falling	CrCb7	CrCb6	CrCb5	CrCb4	falling	Y7	Y6	Y5	Y4

2   **Table 1 (single color) – VIDBus Formats**

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Video stream A   Video stream B

line	C(U)	7	6	5	4	3	2	1	0
word 0	rising	CrCb3	CrCb2	CrCb1	CrCb0	Y3	Y2	Y1	Y0
word 1	falling	CrCb7	CrCb6	CrCb5	CrCb4	Y7	Y6	Y5	Y4

6   **Table 2 (single color/single monochrome) – VIDBus Formats**

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8   When configured as a color bus, the upper and lower halves of the VID bus transfers

9   16 bits of video data during each clock period (8 bits on the rising edge and 8 bits on the

10   falling edge). Eight of the bits represent the intensity data for a pixel (Y0-7), and the other

11   eight bits represent half of the pixel color data. The color data alternates on successive

12   transfers between Cr and Cb. Thus, in transferring 32 bits of video data, two pixel intensity

13   values are transferred, but only one complete set of color values are transferred (8 bits of Cr

14   and 8 bits of Cb).

15   The multiplexed data is illustrated for both color and monochrome. In an alternative

16   system having several buses, several buses could be designated color or single monochrome,

17   with the primary intention of using the system for color but with the capability of transmitting

18   in a single monochrome source, thereby saving one clock pin per bus.

19   Video control signals are imbedded in the pixel data so that only eight data bits are

20   required to completely define the video signal. In an example embodiment, certain Y values

21   in combination with CrCb values are used for frame control information. For example,

22   predetermined Y values can be used to indicate an invalid pixel, the end of a pixel line,

23   horizontal and vertical resets of blank and active lines etc. Table 3 illustrates the control

24   codes that are used to define a color video signal while Table 4 illustrates the control codes

25   that are used to define a monochrome video signal.

26   Y Value   Chroma Value   Meaning

Y Value	Chroma Value	Meaning
0x00	0xFF	Invalid pixel; last valid pixel was Cb
	0xFE	Invalid pixel; last valid pixel was Cr

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0x01	0xFF	Cb pixel; last pixel was the last active pixel of the line
	0xFE	Cr pixel; last pixel was the last active pixel of the line
0x02	0xFF	Cb pixel; next pixel is the first active pixel of the line
	0xFE	Cr pixel; next pixel is the first active pixel of the line
0x03	0xFF	Cb pixel; Horizontal Reset of a vertical active line
	0xFE	Cr pixel; Horizontal Reset of a vertical active line
0x04	0xFF	Cb pixel; Horizontal Reset of a vertical blank line
	0xFE	Cr pixel; Horizontal Reset of a vertical blank line
0x05	0xFF	Cb pixel; Vertical Reset followed by an even field
	0xFE	Cr pixel; Vertical Reset followed by an even field
0x06	0xFF	Cb pixel; Vertical Reset followed by an odd field
	0xFE	Cr pixel; Vertical Reset followed by an odd field
0x07 to 0x0F	0xFF 0xFE	Unused codes

Table 3 – Color Video Control Codes

Y Value	Meaning
0x00	Invalid pixel
0x01	Last pixel was the last active pixel of the line
0x02	Next pixel is the first active pixel of the line
0x03	Horizontal Reset of a vertical active line
0x04	Horizontal Reset of a vertical blank line
0x05	Vertical Reset followed by an even field – large frame
0x06	Vertical Reset followed by an odd field – large frame
0x07	Vertical Reset followed by an even field – small frame *
0x08	Vertical Reset followed by an odd field – small frame *
0x09 to 0x0F	Unused
0x10 to 0xFF	Valid pixel
	* These codes used for digital radar video only

Table 4 – Monochrome Video Control Codes

Each of bus drivers 0-4, implemented for example, using 74ADT2244A bus drivers from Texas Instruments, buffers output data from controller 204 and drives a respective one of buses 0-4. It will be appreciated that buses 0-4 comprise video bus 158 of FIG. 2. Buses 0-2 are each comprised of 14 signal lines, and buses 3 and 4 are each comprised of 11signals lines. The 14 signal lines driven by a bus driver include 4 lines for accommodating in

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1   addition to the 10 data lines, triplicate drivers for clock signal integrity and accommodate the

2   number of slots in the backplane.

3   Digitizer 152 also includes channels for receiving input digital video data, formatting

4   the video data for VIDbus2, and selecting desired video data. For example, digital video

5   receivers 208 and 210 are provided for receiving video data and converting to VIDbus2

6   format and are implemented using FPGAs. A third digital video input channel 211 is

7   provided for receiving pre-formatted VIDbus2 video data. For example, reduced-frame rate

8   video data may be input to digital source video controller 212.

9   Analog source video controller 204 performs the routing of signals from digitizers 0-4

10   to the proper one of video buses 0-4. The video streams that are output and the buses 0-4 on

11   which the streams are driven are selected by controller 204 in response to control signals

12   received via interface and control logic 220. As noted above, two monochrome video streams

13   can be selectively multiplexed on one of the 10-bit lines, or one 10-bit line can be used for a

14   color video stream in accordance with control signals received via control logic 220.

15   Digital source video controller 212 receives video data from the digital sources, and in

16   response to control signals received via VME interface and control logic 220, selects from the

17   sources data to be driven on buses 2-4. Both controllers 204 and 212 are implemented using

18   FPGAs in the example embodiment.

19   Digitizer 152 is coupled to VME bus 160 via interface and control element 220.

20   Digitizer 152 operates as an 8-bit slave on VME bus 160, and control logic 220 conforms to

21   the standard ANSI/VITA1-1994 as implemented on an FPGA. Analog source controller 204

22   and digital source controller 212 receive control signals via control logic 220 that indicate

23   which video streams are to be output on which video buses 0-4.

24   Bus controller 228 provides an interface between interface and control logic 220 and

25   digitizers 0-4. Each of digitizers 0-4 has a serial input configuration port, through which

26   configuration data can be loaded into configuration registers. The data in a configuration

27   register dictates, which of the input video signals is selected for digitization by a digitizer.

28   Video test generator 230 provides test input video signals to digitizer 0-4, for example,

29   solid, vertical stripes, horizontal stripes, and checkerboard patterns. Controller 212 is

30   connected to test generator 230 to select which image is output and provided to digitizers 0-4.

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1   FIG. 4 is a functional block diagram of a fail-safe video module in accordance with

2   one embodiment of the invention. Fail-safe video module 156 independently selects either

3   the output video signal from terminal controllers 154-1 - 154-n or a video signal from one of a

4   plurality of fail-safe video sources and provides as output RGB video signals to a plurality of

5   display terminals. A set of relays is used to pass video signals, even when the module is not

6   energized.

7   The fail-safe video signals are input to multiplexer-and-relay module 250 on line 164

8   (referenced as fail-safe signals 0-m), and the video signals from the terminal controllers are

9   input to module 250 on line 252. The output video signal on line 254 is referred to as the

10   output of station 0 of module 250. The station 0 output signal is either fail-safe signal 0 or in

11   the video signal from terminal controller 0 (154-1 in FIG. 2). The output video signal on line

12   256 is from a last one of the multiplexers of module 250 and is either one of fail-safe signals

13   1-m or the video signal from one of the terminal controllers. A group of output video signals

14   is illustrated by line 258. The signals on line 258 are the output video signals of stations 1-

15   (m-1) of the multiplexer and relay module 250. FIGs. 5, 6, and 7 further illustrate the stations

16   implemented in the multiplexer and relay module 250.

17   The multiplexers and relays (not shown) of module 250 are controlled via line 271 by

18   signals from VME interface and control logic element 270, which is coupled to VME control

19   bus 160. A processor (not shown) connected to control bus 160 in accordance with

20   application-specific programming, addresses fail-safe module 156 and writes control words to

21   registers (not shown) within logic element 270. The control words in the control registers

22   (one control register per station) controls the selection signals of line 271. In the example

23   embodiment, logic element 270 is implemented with an FPGA.

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25   FIG. 5 is a circuit schematic for one color (e.g., of RGB) of station 0 of multiplexer-

26   and-relay module 250, which is in an energized state. While not shown, it will be appreciated

27   that station 0 includes comparable circuitry for the other two colors. Station 0 passes either

28   the video signal from a terminal controller (e.g., 154-1) or the video signal from fail-safe

29   video source 0 (not shown).

30   Relay 0A receives the video signal from the terminal controller, and relay 0B receives

31   the video signal from the fail-safe source. When the multiplexer-and-relay module is in an

1   energized state, relay 0A passes the video signal from the terminal controller to the connected

2   display terminal, and relay 0B passes the input video signal to a terminated connection (e.g., a

3   75 ohm termination). When module 250 is in a non-energized state, relay 0A passes the video

4   signal from the terminal controller to a terminated connection, and relay 0B passes the fail-

5   safe signal to the display terminal.

6   Select signals are provided on lines 502 and 504 from control logic element 270 to

7   relays 0A and 0B to select to which terminals of the relays the input video signal is routed

8   when the relays are in energized and non-energized states. In accordance with one example

9   embodiment, the relays are implemented using ER134M4-5A relays from Teledyne, Inc.

10

11   FIGs. 6A and 6B are circuit schematics for one color (of RGB) of stations 1-8 of an

12 example multiplexer-and-relay module 250 having 9 stations and which is in an energized

13 state. It will be appreciated that comparable circuitry (not shown) is implemented for each of

14 the other two colors. While 9 stations are illustrated (station 0 in FIG. 5 and stations 1-8 in

15 FIGs. 6A and 6B), it will be appreciated that various other station configurations can be

16 implemented depending upon the number of terminal controllers and number of fail-safe

17 video sources. When multiplexer-and-relay module 250 is in an energized state, stations 1-7

18 output either a respective one of the video signals from the connected terminal controllers or a

19 selected one of the video signals from fail-safe sources 1-7. When multiplexer-and-relay

20 module 250 is in an non-energized state, stations 1-7 output a respective one of the video

21 signals from a connected one of the fail-safe sources. Station 8 outputs the video signal from

22 a selected one of the fail-safe sources 1-7 only when multiplexer-and-relay module 250 is in

23 an energized state.

24   Stations 1-7 each include respective multiplexers 601-607. Each of the multiplexers

25 receives a video signal from a respective terminal controller along with the video signals from

26 7 fail-safe sources. Dedicated selection signals are provided to each of the multiplexers for

27 independent selection of a video signal. For example, the video signal from the terminal

28 controller connected to station 1 can be selected at station 1, and the video signal from fail-

29 safe source 1 can be selected at station 7. The selection signals are driven by control section

30 270 of multiplexer-and-relay module 250, which is controlled by an external processor via

31 control bus 160.

1   Stations 1-7 also include a pair of respective relays 1A-7A and 1B-7B. Each "A"

2   relay is connected to receive a video signal from one of the fail-safe sources 1-7. For

3   example, relay 2A receives the video signal from fail-safe source 2. When in an energized

4   state, the "A" relays pass the input video signals to the multiplexers of stations 1-7, as

5   selected by the select signal input to the relays. For example, the video signal from fail-safe

6   source 1 is output from relay 1A, buffered, and routed on signal line 621 to multiplexers 601-

7   608. Similarly, video signals from fail-safe sources 2-7 are provided by relays 2A-7A and

8   carried on lines 622-627 to multiplexers 601-608. When the "A" relays are in a non-

9   energized state, the video signals are passed to the associated "B" relays instead of the

10   multiplexers.

11   Each "B" relay has two input ports: one connected to the output of a respective one of

12   the multiplexers 1-7, and the other connected to an output port of an "A" relay which passes

13   the input video signal when the "A" relay is in a non-energized state. For example, relay 2B

14   is coupled to the output port of multiplexer 602 and to one of the output ports of relay 2A.

15   When multiplexer-and-relay module 250 is in an energized state, relay 2B passes the video

16   signal selected at multiplexer 602, and when the multiplexer-and-relay module is in a non-

17   energized state, relay 2B passes the video signal passed by relay 2A.

18   Station 8 includes multiplexer 608, but has no associated fail-safe video source.

19   Multiplexer 608 receives input video signals from a terminal controller at port 0 and video

20   signals from the fail-safe sources 1-7 on ports 1-7. The output of station 8 can be used, for

21   example, as input to a frame-grabber.

22   The present invention is believed to be applicable to a variety of applications

23   involving distribution of video signals. Other aspects and embodiments of the present

24   invention beyond those specifically described herein will be apparent to those skilled in the

25   art from consideration of the specification and practice of the invention disclosed herein. It is

26   intended that the specification and illustrated embodiments be considered as examples only,

27   with a true scope and spirit of the invention being indicated by the following claims.